What is claimed is:

1. A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern; and

a terminal which is formed on the molding resin and is connected to the conductive post, wherein

a connecting portion (boundary portion) of the conductive wiring pattern and conductive post is provided with a slit to disperse stress to be applied to the connecting portion.

2. A chip-size semiconductor package according to claim 1, wherein

the connecting portion is provided with a plurality of slits, which are separated from each other.

3. A chip-size semiconductor package according to claim 2, wherein

the slits are shaped to be rectangular and arranged to extend radially.

4. A chip-size semiconductor package according to claim 1, wherein

the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

5. A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is connected to the conductive wiring pattern;

a terminal which is formed on the molding resin and is connected to the conductive post; and

a dummy pattern arranged adjacent a connecting portion (boundary portion) of the conductive post and wiring pattern.

6. A chip-size semiconductor package according to claim 5, wherein

the dummy pattern is a conductive pattern which is formed in the same process as the conductive wiring pattern and is arranged parallel to the conductive wiring pattern.

7. A chip-size semiconductor package according to claim 5, wherein

the dummy pattern comprises two parts arranged at the both side of the conductive pattern.

8. A chip-size semiconductor package according to claim 7, wherein

the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern,

the two parts of the dummy pattern are arranged along the conductive post and conductive wiring pattern.

9. A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is

connected to the conductive wiring pattern; and

a terminal which is formed on the molding resin and is connected to the conductive post, wherein

at least one of the conductive wiring pattern and conductive post is provided with a dent around a connecting portion (boundary portion) of the conductive wiring pattern and conductive post.

10. A chip-size semiconductor package according to claim 9, wherein

the dent is shaped to be square.

11. A chip-size semiconductor package according to claim 9, wherein

the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

12. A chip-size semiconductor package, comprising:

a semiconductor chip;

a metal pad formed on the semiconductor chip;

a wafer coat formed over the semiconductor chip;

a conductive wiring pattern formed on the wafer coat, in which the metal pad is electrically connected to the conductive pattern;

a molding resin formed over the conductive wiring pattern;

a conductive post which is formed in the molding resin and is

connected to the conductive wiring pattern; and

a terminal which is formed on the molding resin and is connected to the conductive post, wherein

the conductive wiring pattern is shaped to have a first region extending outwardly from the conductive post and a second region extending vertically from the first region.

13. A chip-size semiconductor package according to claim 12, wherein

the second region comprises a plurality of projecting parts each of which extends vertically from the first region.

14. A chip-size semiconductor package according to claim 13, wherein

the projecting pats of the second region are extended from both sides of the first region.

15. A chip-size semiconductor package according to claim 12, wherein

the connecting portion is shaped to decrease in area gradually from the conductive post to the conductive wiring pattern.

16. A chip-size semiconductor package according to claim 15, wherein

at least one of the projecting pats forms a part of the conductive post.

17. A semiconductor device, comprising:

a semiconductor chip;

a pad which is formed on said semiconductor chip;

an insulating film which is formed on said semiconductor chip;

a conductive portion which is electrically connected to said pad, wherein

said conductive portion comprises:

a first portion which is formed on said insulating film and said pad; and

a second portion which is formed on said insulating film, wherein said second portion has a connection part contacting with said first portion formed on said insulating film, wherein said contacting part is gradually narrow toward said first portion.